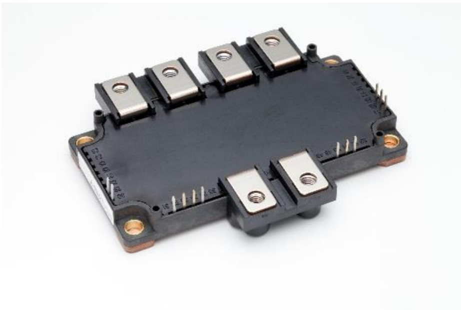
MITSUBISHI ELECTRIC

<Full-SiC Modules>

FMF800DX-24A

HIGH POWER SWITCHING USE
INSULATED TYPE



dual switch (Half-Bridge)

Drain current I_D .... 8 0 0 A
Drain-Source voltage V_{DSX} .... 1 2 0 0 V
Maximum junction temperature T_{vjmax} .... 1 5 0 °C

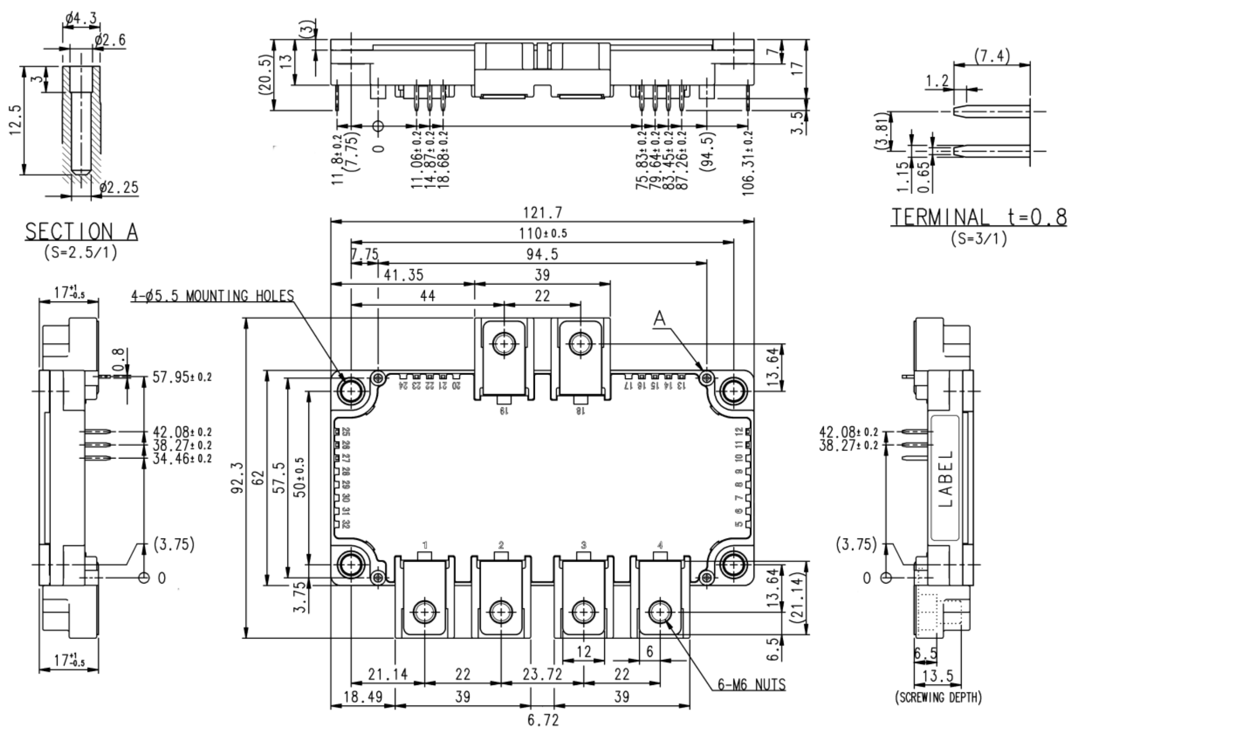
- ●Silicon Carbide MOSFET + Silicon Carbide Schottky Barrier Diode
- ●Flat base Type
- ●Copper base plate
- ●RoHS Directive compliant
- ●Recognized under UL1557, File E323585

APPLICATION

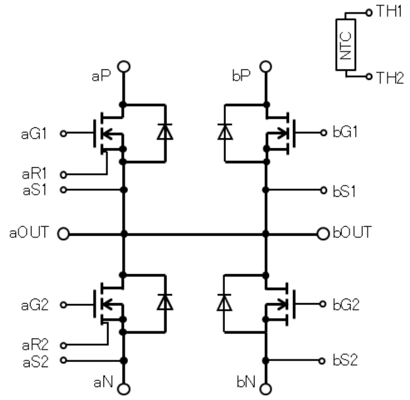
AC Motor Control, Motion/Servo Control, Power supply, etc.

OUTLINE DRAWING & INTERNAL CONNECTION

Dimension in mm



INTERNAL CONNECTION



Terminal code

1	aP
2	aN
3	bN
4	bP
11	bG1
12	bS1
13	TH2
14	TH1
15	bG2
16	bS2
18	bOUT
19	aOUT
21	aS2
22	aR2
23	aG2
25	aS1a
26	aR1
27	aG1

Tolerance otherwise specified

Division of Dimension			Tolerance
0.5	to	3	±0.2
over 3	to	6	±0.3
over 6	to	30	±0.5
over 30	to	120	±0.8
over 120	to	400	±1.2

aP and bP, aN and bN should be connected externally.

aR1, aR2 are terminal for drain current sensing. The ratio of aR1/aS1, aR2/aS2 is approximately 1:61500.

MAXIMUM RATINGS (T_{vj}=25 °C, unless otherwise specified)

Symbol	Item	Conditions	Rating	Unit
V_{DSX}	Drain-source voltage	V_{GS}=-15 V	1200	V
V_{GSS}	Gate-source voltage	D-S short-circuited	± 20	V
I_D	Drain current	DC	800	A
I_{DRM}		Pulse, Repetitive, T_{vj}=150℃ (Note.3)	1600	
P_{tot}	Total power dissipation	T_C=25 °C (Note.2, 4)	2975	W
I_S (Note.1)	Source current	DC	800	A
I_{SRM} (Note.1)		Pulse, Repetitive, T_{vj}=150℃ (Note.3)	1600	
V_{isol}	Isolation voltage	Terminals to base plate, RMS, f=60 Hz, AC 1 min	4000	V
T_{vjmax}	Maximum junction temperature	Instantaneous event (overload)	150	°C
T_{Cmax}	Maximum case temperature	(Note.2)	125	
T_{vjop}	Operating junction temperature	Continuous operation (under switching)	-40 ~ +150	
T_{stg}	Storage teperature	-	-40 ~ +125	

ELECTRICAL CHARACTERISTICS (T_{vj}=25 °C, unless otherwise specified)

Symbol	Item	Conditions (note10)		Limits Min.	Typ.	Max.	Unit
I_{DSX}	Drain-source cut-off current	V_{DS}=V_{DSX}, V_{GS}=-15V		-	-	44	mA
		V_{DS}=800V, V_{GS}=-15V		-	-	1	
I_{GSS}	Gate-source leakage current	V_{GS}=V_{GSS}, D-S short-circuited		-	-	0.5	μA
$V_{GS(th)}$	Gate-source threshold voltage	I_D=271 mA, V_{DS}=10 V		0.5	1	1.6	V
$r_{DS(on)}$ (chip)	Static drain-source On-state resistance	I_D=800 A, V_{GS}=15 V (Note.6)	T_{vj}=25 °C	-	1.6	-	mΩ
			T_{vj}=150 °C	-	2.8	-	
$V_{DS(on)}$ (chip)	Static drain-source On-state voltage	I_D=800 A, V_{GS}=15 V	T_{vj}=25 °C	-	1.3	-	V
			T_{vj}=125 °C	-	2.02	-	
			T_{vj}=150 °C	-	2.2	-	
$V_{DS(on)}$ (terminal)	Static drain-source On-state voltage	I_D=800 A, V_{GS}=15 V (Note.6)	T_{vj}=25 °C	-	1.66	2.3	V
			T_{vj}=125 °C	-	2.38	-	
			T_{vj}=150 °C	-	2.56	-	
C_{iss}	Input capacitance	V_{DS}=10 V, V_{GS}=0V		-	75	-	nF
C_{oss}	Output capacitance			-	25	-	
C_{rss}	Reverse transfer capacitance			-	2	-	
Q_G	Gate charge	V_{DD}=600 V, I_D=800 A, V_{GS}=0→15 V		-	2800	-	nC
$t_{d(on)}$	Turn-on delay time	V_{DD}=600 V, I_D=800 A, V_{GS}=±15 V, R_G=2.2Ω, Inductive load		-	120	-	ns
t_r	Rise time			-	80	-	
$t_{d(off)}$	Turn-off delay time			-	420	-	
t_f	Fall time			-	60	-	
Q_C	Drain-source charge			-	4	-	μC
V_{SD} (Note.1) (chip)	Source-drain voltage	I_S=800 A (Note.6), V_{GS}=-15 V,	T_{vj}=25 °C	-	1.7	-	V
			T_{vj}=125 °C	-	2.2	-	
			T_{vj}=150 °C	-	2.4	-	
V_{SD} (Note.1) (terminal)	Source-drain voltage	I_S=800 A (Note.6), V_{GS}=-15 V,	T_{vj}=25 °C	-	2.05	2.45	V
			T_{vj}=125 °C	-	2.55	-	
			T_{vj}=150 °C	-	2.75	-	
E_{on}	Turn-on switching energy per pulse	V_{DD}=600 V, I_D/I_S=800 A, V_{GS}=±15 V, R_G=2.2Ω, T_{vj}=125 °C, Inductive load		-	22	-	mJ
E_{off}	Turn-off switching energy per pulse			-	40	-	
E_{rec} (Note.1)	Diode switching energy per pulse			-	0.8	-	
$R_{DD'+SS'}$	Internal lead resistance	P-N, T_C=25 °C (Note.2)		-	0.5	-	mΩ
r_g	Internal gate resistance	per Tr1 chips total, per Tr2 chips total (internal connection in page 5.)		-	0.54	-	Ω
L_s	Internal stray inductance	P-N		-	10	-	nH
V_s	Current sensor output voltage	I_D=1600 A, V_{GS}=±15 V, R_S=22 Ω, T_{vj}=150 °C		-	0.7	-	V

Caution; No short-circuit capability is designed.

THERMAL RESISTANCE CHARACTERISTICS

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Thermal resistance (Note.2)	Junction to case, per Tr1 chips total, per Tr2 chips total (internal connection in page 5.)	-	-	42	K/kW
$R_{th(j-c)D}$		Junction to case, per Di1 chips total, per Di2 chips total (internal connection in page 5.)	-	-	61	
$R_{th(c-s)}$	Contact thermal resistance (Note.2)	Case to heat sink, Thermal grease applied (Note.8)	-	15	-	K/kW

NTC THERMISTOR PART

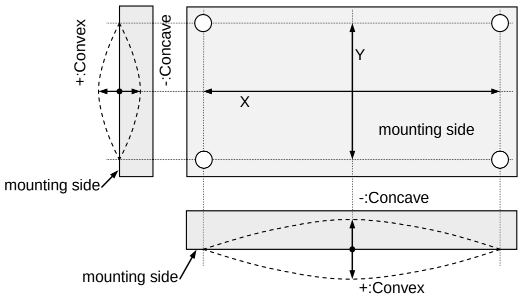
Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
R_{25}	Zero-power resistance	T_C=25 °C (Note.2)	4.85	5.00	5.15	kΩ
ΔR/R	Deviation of resistance	T_C=100 °C, R_{100}=493 Ω (Note.2)	-7.3	-	+7.8	%
$B_{(25/50)}$	B-constant	Approximate by equation (Note.7)	-	3375	-	K
P_{25}	Power dissipation	T_C=25 °C (Note.2)	-	-	10	mW

MECHANICAL CHARACTERISTICS

Symbol	Item	Conditions		Limits			Unit
				Min.	Typ.	Max.	
M_t	Mounting torque	Main terminals	M 6 screw	3.5	4.0	4.5	N·m
M_s		Mounting to heat sink	M 5 screw	2.5	3.0	3.5	
d_s	Creepage distance	Terminal to terminal		12	-	-	mm
		Terminal to base plate		13.6	-	-	
d_a	Clearance	Terminal to terminal		10	-	-	mm
		Terminal to base plate		12.3	-	-	
m	mass	-		-	390	-	g
e_c	Flatness of base plate	On the centerline X, Y (Note.5)		±0	-	+100	μm

*: This product is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU.

Note1. Represent ratings and characteristics of the anti-parallel, source-drain free wheeling diode (FWD).
2. Case temperature (T_C) and heat sink temperature (T_s) are defined on the each surface (mounting side) of base plate and heat sink just under the chips. Refer to the figure of chip location.
3. Pulse width and repetition rate should be such that the device junction temperature (T_{vj}) dose not exceed T_{vjmax} rating.
4. Junction temperature (T_{vj}) should not increase beyond T_{vjmax} rating.
5. The base plate (mounting side) flatness measurement points (X, Y) are as follows of the following figure.



6. Pulse width and repetition rate should be such as to cause negligible temperature rise. Refer to the figure of test circuit.
7. $B_{(25/50)} = \ln(\frac{R_{25}}{R_{50}})/(\frac{1}{T_{25}} - \frac{1}{T_{50}})$

   R_{25}: resistance at absolute temperature T_{25} [K]; T_{25}=25 [°C]+273.15=298.15 [K]

   R_{50}: resistance at absolute temperature T_{50} [K]; T_{50}=50 [°C]+273.15=323.15 [K]
8. Typical value is measured by using thermally conductive grease of λ=0.9 W/(m·K).
9. Use the following screws when mounting the printed circuit board (PCB) on the standoffs.
   "φ2.6×10 or φ2.6×12, B1 tapping screw"
   The length of the screw depends on the thickness (t1.6) of the PCB.
10. Per switch (ex. Tr1 chips total in page.5)

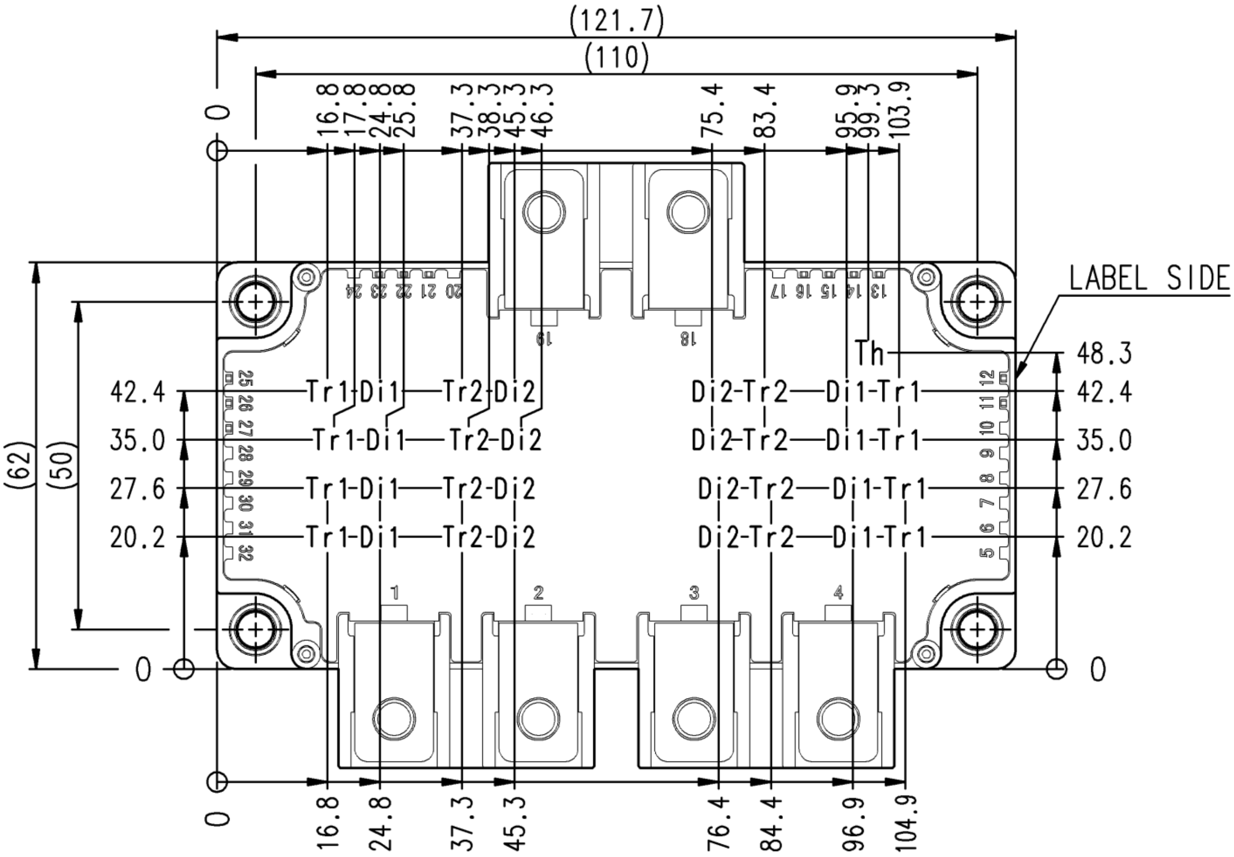
RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	(DC) Supply voltage	Applied across aP/bP-aN/bN	-	600	850	V
$V_{GS(+)}$	Gate (-source drive) voltage (positive)	Applied across aG1-aS1/bG1-bS1/ aG2-aS2/bG2-bS2	13.5	15	16.5	V
$V_{GS(-)}$	Gate (-source drive) voltage (negative)	Applied across aG1-aS1/bG1-bS1/ aG2-aS2/bG2-bS2	-16.5	-15.0	-9	V
R_G	External gate resistance (Note.11)	Per switch	1.6	-	10	Ω

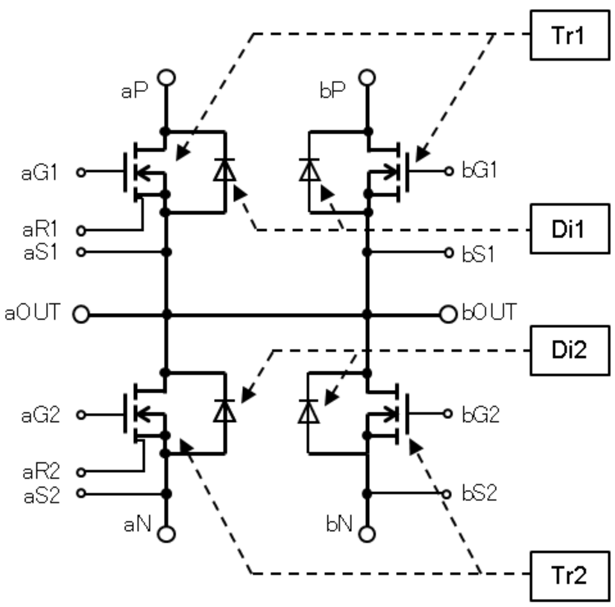
Note 11. The value of external gate resistance should be considered the surge voltage not to exceed the rating voltage in the worst system condition.

CHIP LOCATION (Top view)

Dimension in mm, tolerance: ±1 mm



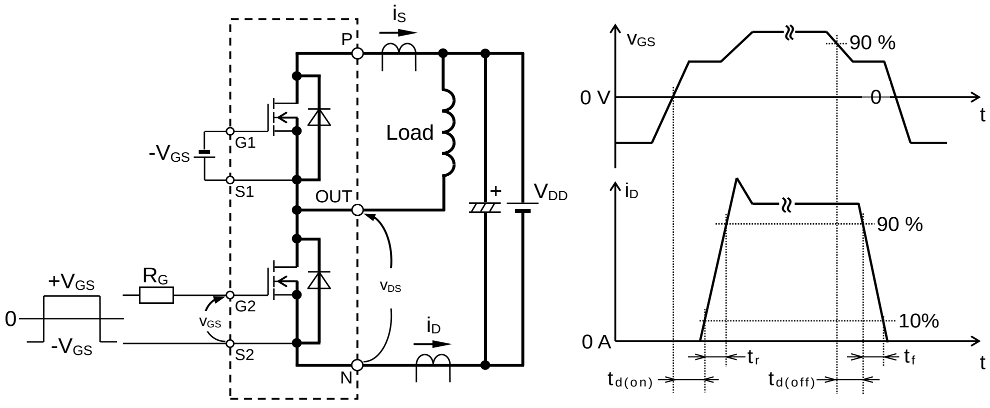
Tr1/Tr2: SiC-MOS, Di1/Di2: SiC-SBD, Th: NTC Thermistor



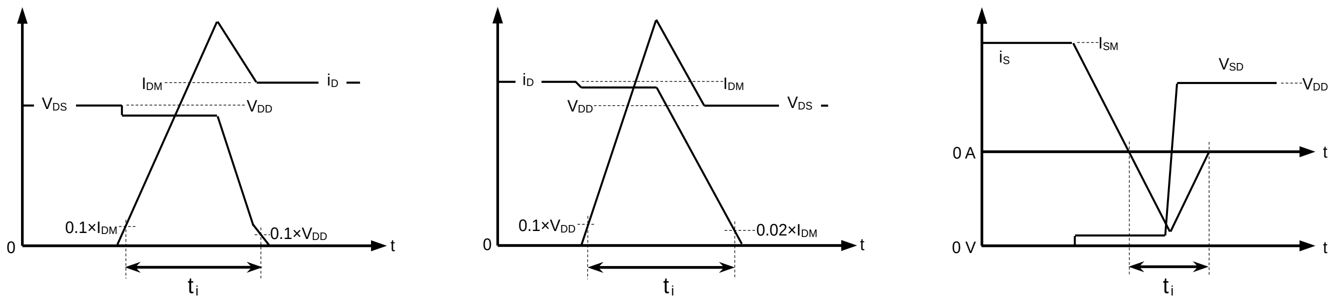
- The terminal aP-bP, aN-bN, aOUT-bOUT must be connected with each other.
- When the current sensor is not used, aR1-aS1, aR2-aS2 must be short-circuited.

Internal connection

TEST CIRCUIT AND WAVEFORMS



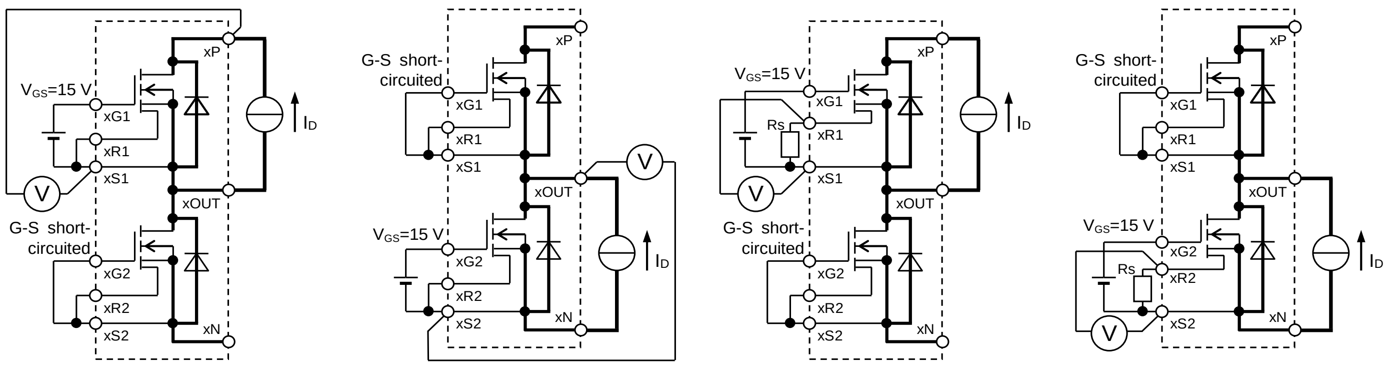
Switching test circuit and waveforms



MOSFET Turn-on switching energy MOSFET Turn-off switching energy DIODE switching energy

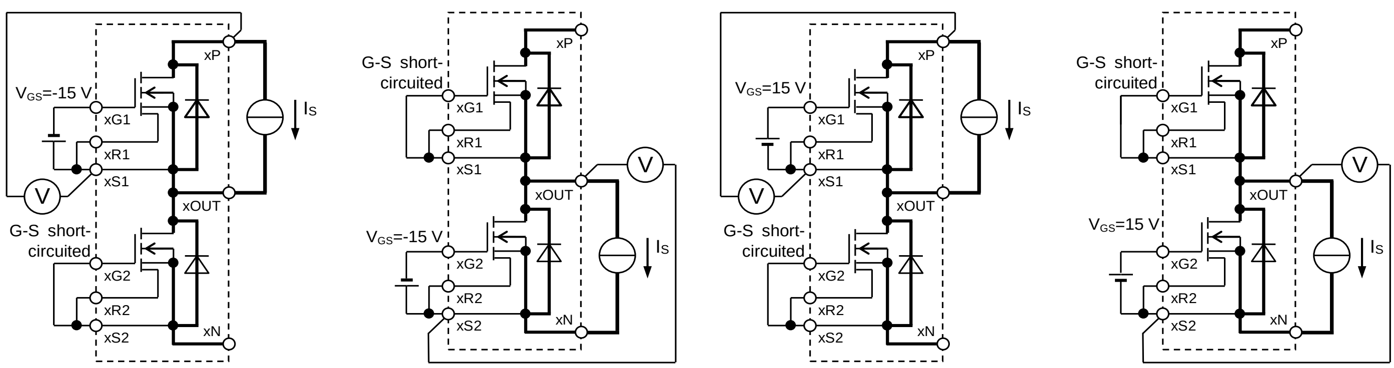
Turn-on / Turn-off switching energy and diode switching energy test waveforms (Integral time instruction drawing)

TEST CIRCUIT



Tr1 Tr2 Tr1 Tr2

$V_{DS(on)}$ test circuit (x: Connected *a and *b) V_S test circuit (x: Connected *a and *b)



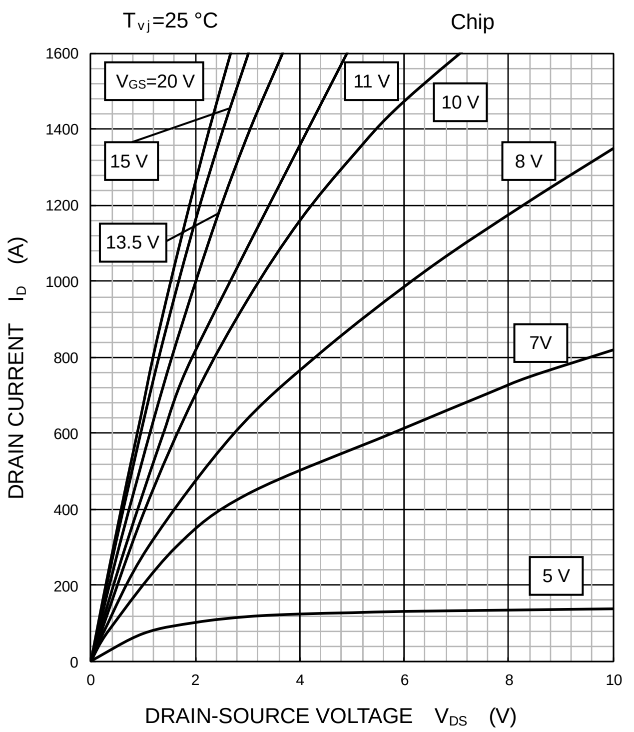
Di1 Di2 Tr1&Di1 Tr2&Di2

V_{SD} test circuit, V_{GS}=-15V (x: Connected *a and *b) V_{SD} test circuit, V_{GS}=15V (x: Connected *a and *b)

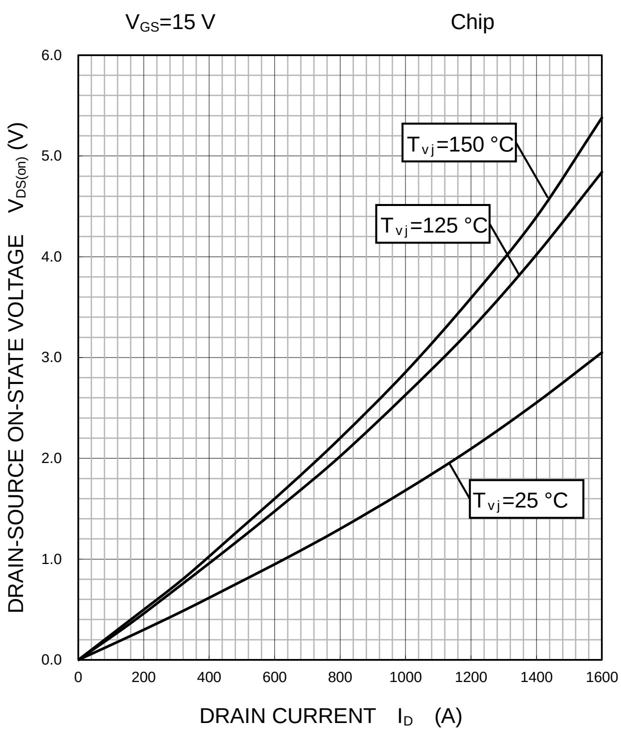
Note: The characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

PERFORMANCE CURVES

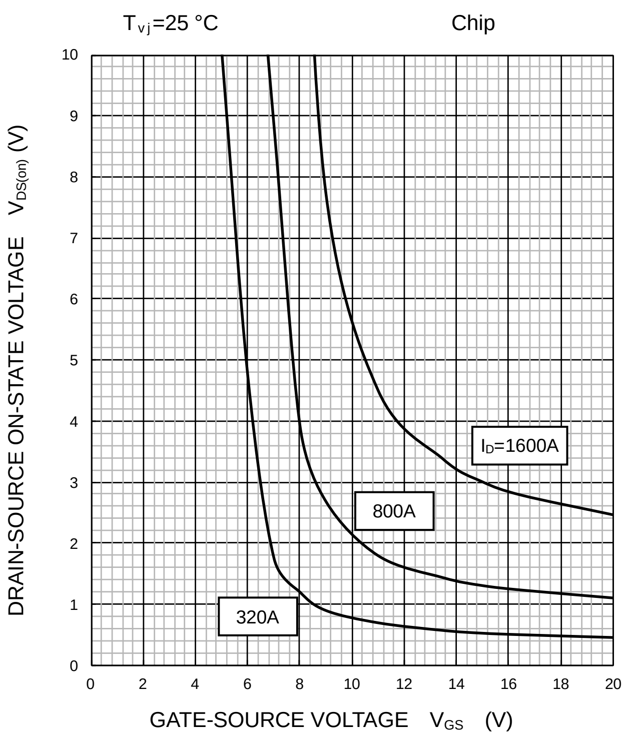
OUTPUT
CHARACTERISTICS
(TYPICAL)



DRAIN-SOURCE ON STATE VOLTAGE
CHARACTERISTICS
(TYPICAL)

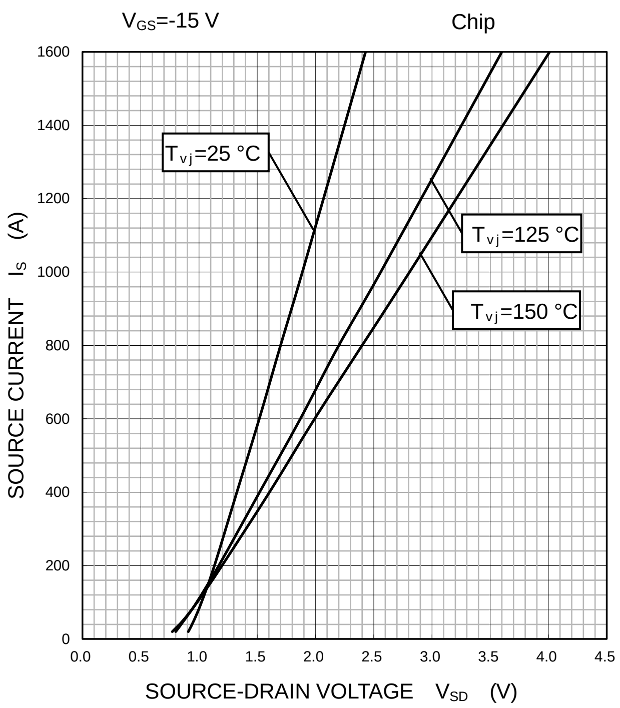


DRAIN-SOURCE ON STATE VOLTAGE
CHARACTERISTICS
(TYPICAL)

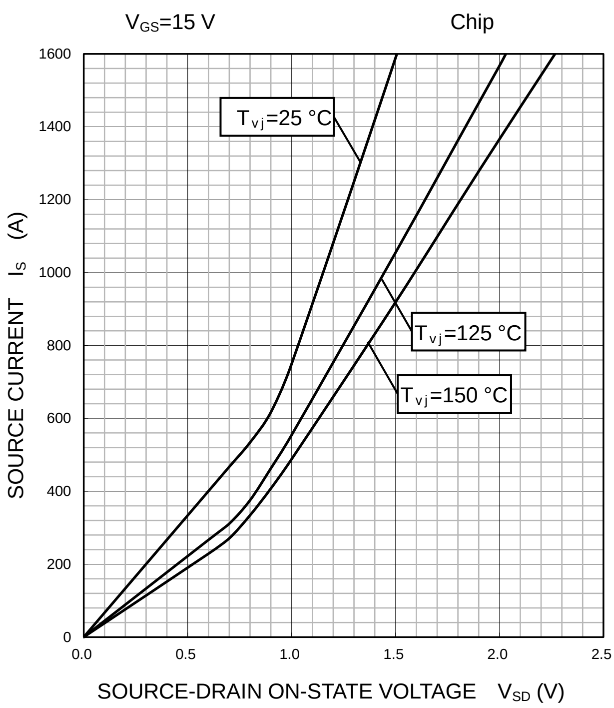


PERFORMANCE CURVES

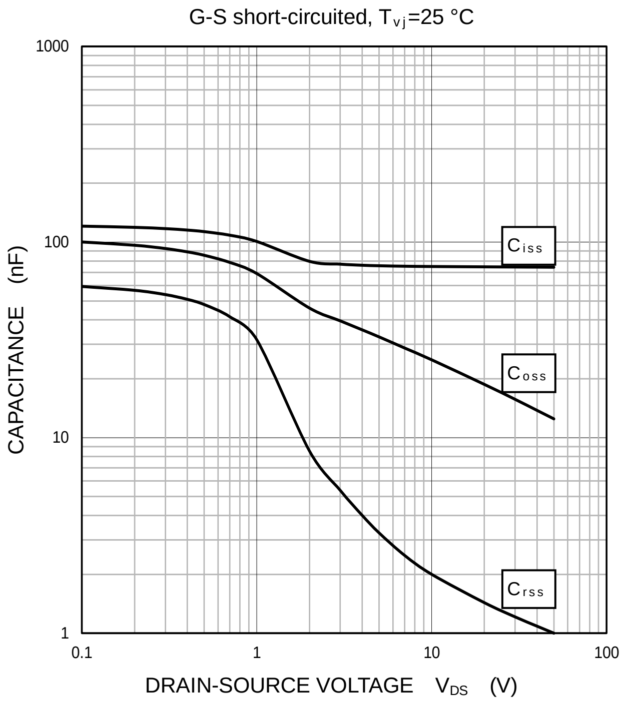
FREE WHEELING DIODE
FORWARD CHARACTERISTICS
(TYPICAL)



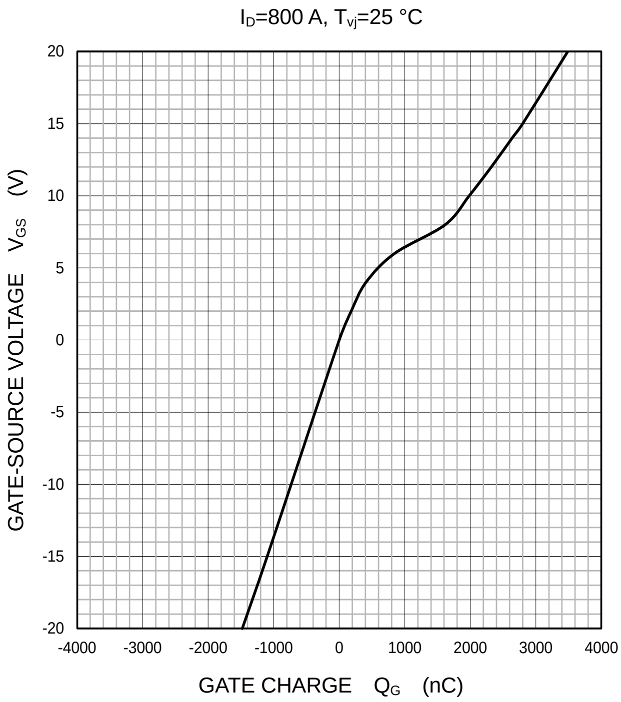
SOURCE-DRAIN ON STATE VOLTAGE
CHARACTERISTICS
(TYPICAL)



CAPACITANCE
CHARACTERISTICS
(TYPICAL)



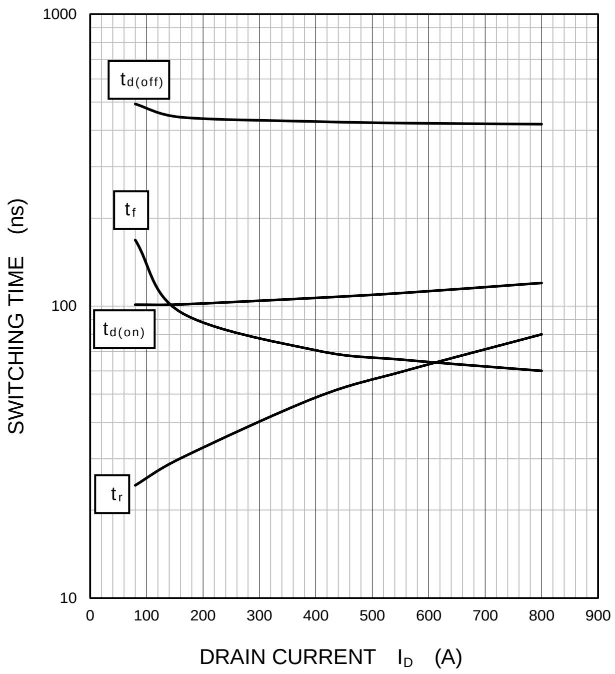
GATE CHARGE
CHARACTERISTICS
(TYPICAL)



PERFORMANCE CURVES

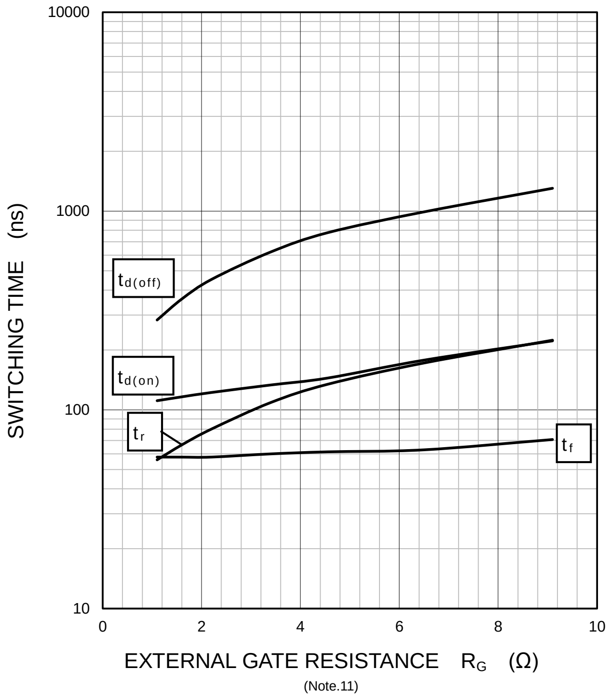
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{DD}=600 V, V_{GS}=±15 V, R_G=2.2Ω,
T_{vj}=125 °C, INDUCTIVE LOAD



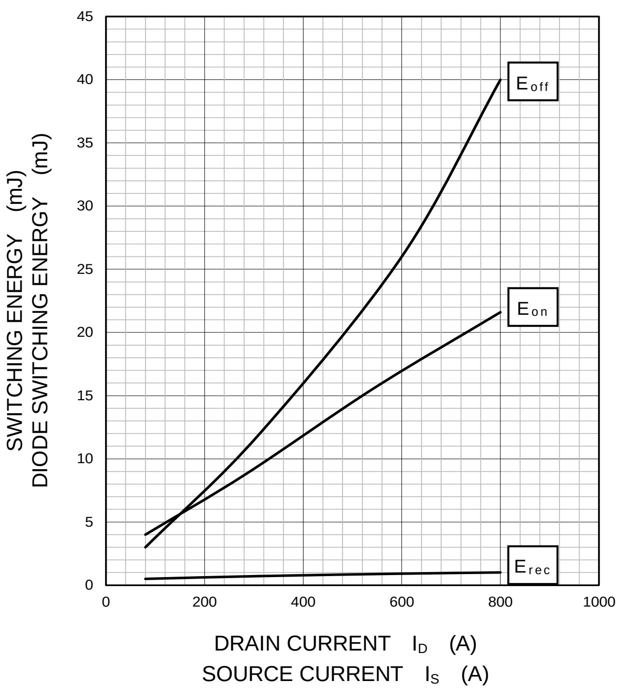
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{DD}=600 V, V_{GS}=±15 V, I_D=800 A,
T_{vj}=125 °C, INDUCTIVE LOAD



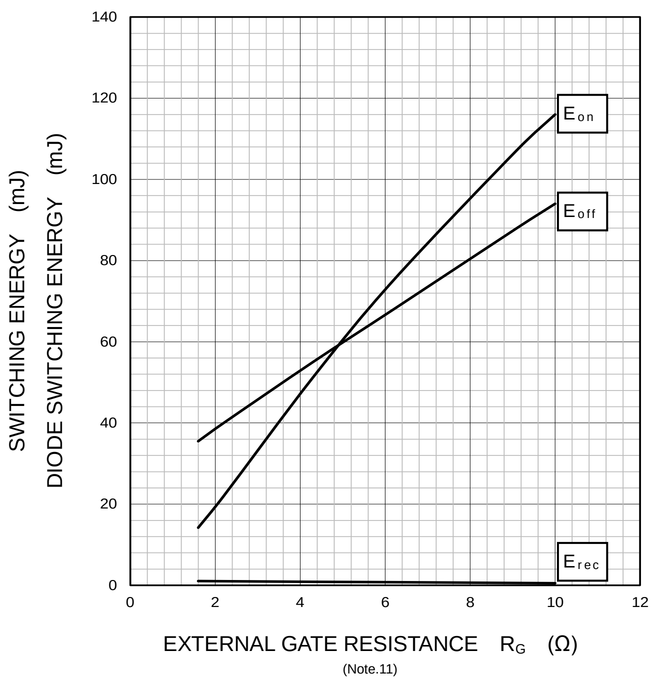
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{DD}=600 V, V_{GS}=±15 V, R_G=2.2Ω, T_{vj}=125 °C,
INDUCTIVE LOAD, PER PULSE



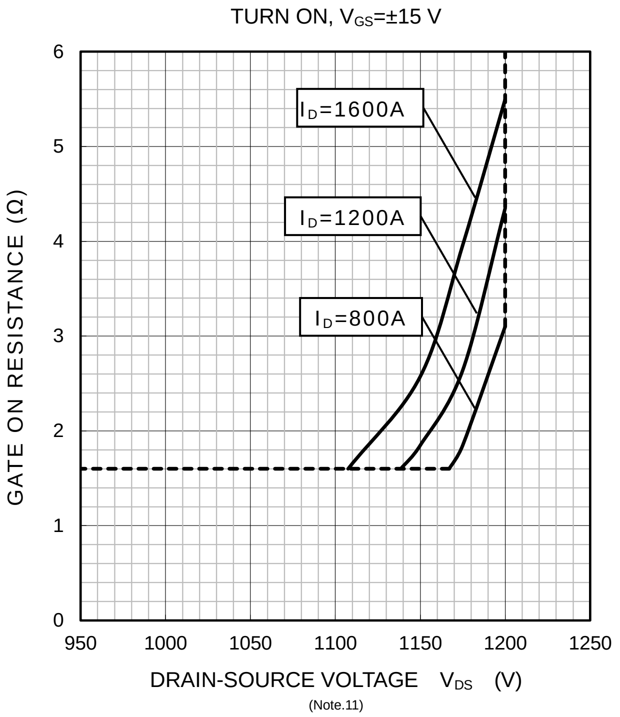
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{DD}=600 V, V_{GS}=±15 V, I_D/I_S=800 A, T_{vj}=125 °C,
INDUCTIVE LOAD, PER PULSE

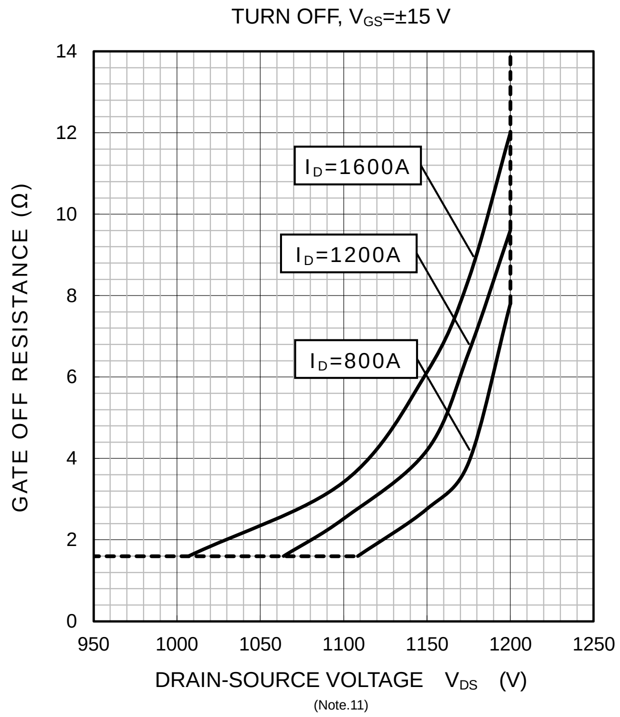


PERFORMANCE CURVES

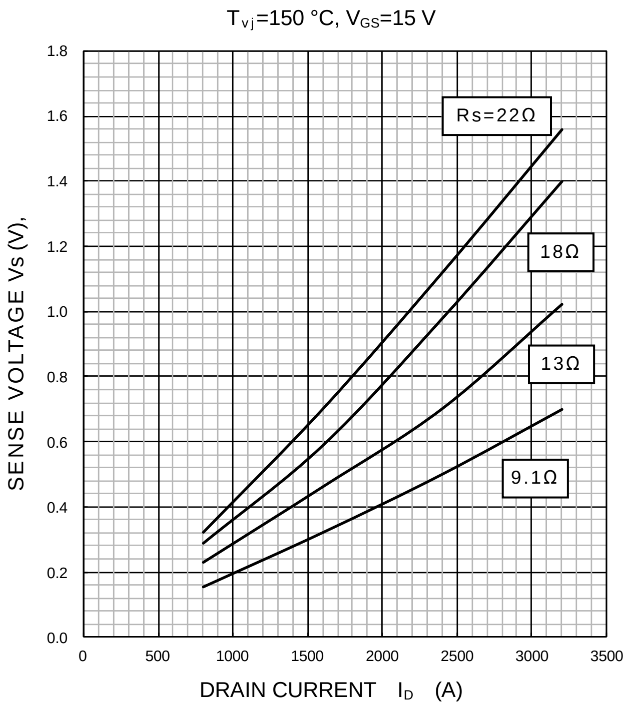
RECOMMENDED GATE RESISTANCE
(MINIMUM)



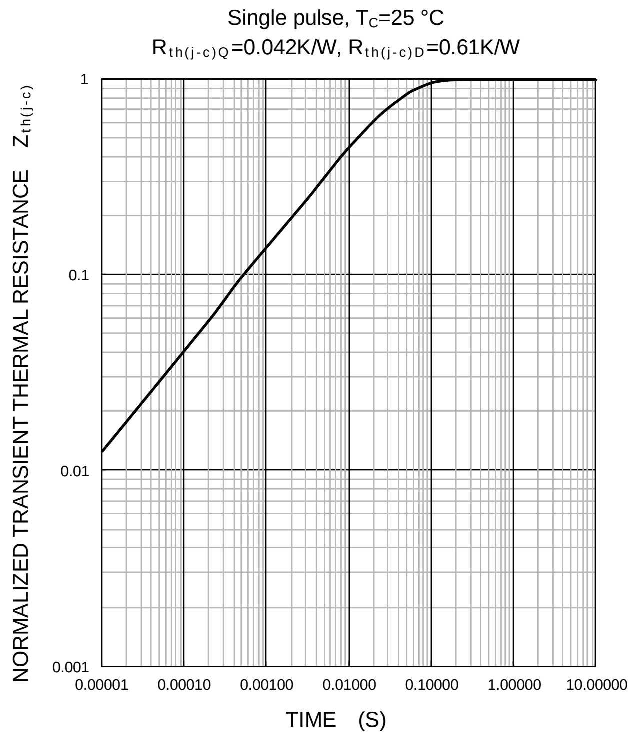
RECOMMENDED GATE RESISTANCE
(MINIMUM)



SENSE VOLTAGE
CHARACTERISTICS
(TYPICAL)



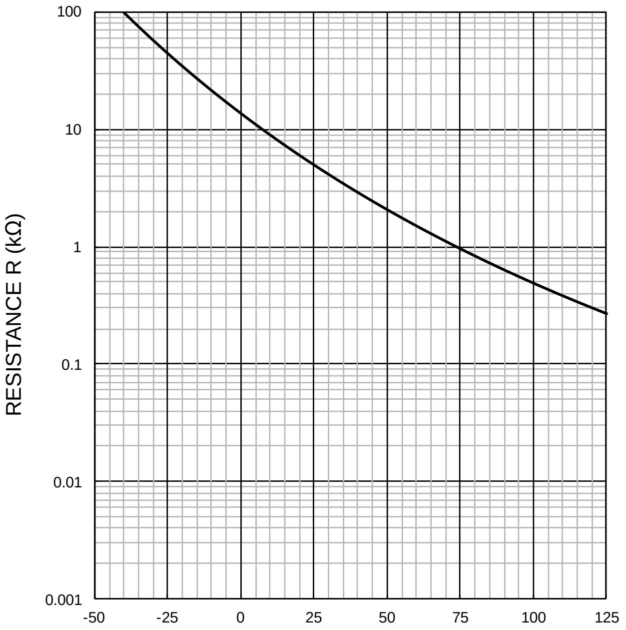
TRANSIENT THERMAL IMPEDANCE
CHARACTERISTICS
(MAXIMUM)



PERFORMANCE CURVES

NTC thermistor part

TEMPERATURE
CHARACTERISTICS
(TYPICAL)



Note: The characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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